Amendments to the Claims

The listing of claims will replace all prior versions, and listings of claims in the application.

1-14. (Canceled)

15. (Original) A circuit, comprising:

a buffer;

a sampling circuit having a switch; and

a damping circuit coupled between the buffer and the sampling circuit;

wherein the damping circuit is adapted to reduce charge glitches when the switch closes.

16. (Original) The circuit of claim 15, wherein the damping circuit comprises a low pass filter.

17. (Original) The circuit of claim 16, wherein the low pass filter is an RC low pass filter.

18. (Currently Amended) ~~The circuit of claim 15,~~ A circuit, comprising:

a buffer;

a sampling circuit having a switch; and

a damping circuit coupled between the buffer and the sampling circuit;

wherein the damping circuit is adapted to reduce charge glitches when the switch closes; and

wherein the buffer ~~comprises:~~ includes

a source-follower transistor adapted to generate an output signal from an input signal[[;]],

a replica transistor adapted to generate a replica signal from the input signal[[;]], and

a level shifting circuit that provides a level-shifted replica signal at a terminal of the source-follower transistor.

19. (New) The circuit of claim 15, wherein the buffer includes a transistor having a source and a body, and wherein the source and the body are coupled to each other to reduce a signal dependent current.

20. (New) The circuit of claim 15, wherein the buffer includes

a transistor having a source; and

a current source coupled between the source and a voltage supply.

21. (New) The circuit of claim 15, wherein the sampling circuit is a switched-capacitor sampling circuit.

22. (New) The circuit of claim 21, wherein the switched-capacitor sampling circuit includes a capacitor having a first node and a second node, and wherein the first node is coupled to the switch and the second node is coupled to an output of the circuit.

23. (New) The circuit of claim 18, wherein at least one of the source-follower transistor and the replica transistor has a source and a body, and wherein the source and the body are coupled to each other to reduce a signal dependent current.

24. (New) The circuit of claim 18, wherein the buffer further includes a current source coupled between a source of the source-follower transistor and a voltage supply.

25. (New) The circuit of claim 18, wherein the buffer further includes a current source coupled between a source of the replica transistor and a voltage supply.

26. (New) The circuit of claim 18, wherein the sampling circuit is a switched-capacitor sampling circuit.

27. (New) The circuit of claim 26, wherein the switched-capacitor sampling circuit includes a capacitor having a first node and a second node, and wherein the first node is coupled to the switch and the second node is coupled to an output of the circuit.

28. (New) The circuit of claim 18, wherein the damping circuit includes a low pass filter.

29. (New) The circuit of claim 28, wherein the low pass filter is an RC low pass filter.

30. (New) The circuit of claim 18, wherein the level shifting circuit is coupled between a source of the replica transistor and a drain of the source-follower transistor.

31. (New) The circuit of claim 18, wherein the terminal of the source-follower transistor is a drain of the source-follower transistor.

32. (New) The circuit of claim 18, wherein the level shifting circuit includes a voltage source coupled between a source of the replica transistor and the terminal of the source-follower transistor.

33. (New) The circuit of claim 18, wherein the level shifting circuit includes a resistor and a current source, and wherein the resistor is coupled between a source of the replica transistor and the terminal of the source-follower transistor.

34. (New) A circuit, comprising:

a buffer including a transistor having a source and a body;

a sampling circuit including a switch; and

a damping circuit coupled between the buffer and the sampling circuit;

wherein the damping circuit is capable of reducing a charge glitch in response to the switch being opened or closed; and

wherein the source and the body of the transistor are coupled to each other to reduce a signal dependent current.